DPSD BIOS ENGINEERING
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DATE: March 12, 2003

TO: DPSD Business Unit

CC: IPG / DPSD BIOS Engineering

FROM: IPG / DPSD BIOS Engineering

SUBJECT: D845PEBT2 Standard BIOS

About This Release

- **BIOS String:** BT84520A.86A.0020.P08.0303110918
- **UNDI PXE Version:** ICH2 PXE 2.1 Build 083

Features/Errata Fixed in This Release

P08-0020

- Change BIOS String
- Fixed S1 issue
- Changed ACPI OEM Revision field for all ACPI tables to contain the BIOS build date as YYYYMMDD. This insures a constantly increasing number for the ACPI OEM revision field.
- Updated Support for alternate SIO part
- Enabled Add-on ROM display mode support.
- Updated Intel Copyright String to 2003
- Updated System Configuration Data.
- Added string translation and correct spelling error on “Aggressive”
- Fixed issue with password with less than 7 characters
- Intel(R) Boot Agent FE v4.1.09
- Activated and Deactivated the Mouse and Keyboard on S1

P07-0016

- Added new strings translation
- Fixed a 48Bit LBA drives accessing issue.
- Fixed a problem with DDR333 not being displayed in CHIPSET CONFIGURATION -- SDRAM Frequency bios setup page.

P06-0015

- Fixed issue of some registers not being saved and restored correctly when running Hyper-Threading Technology Readiness utility.

P06-0014

- Fixed issue where system will not wake from S1 if the keystroke is hit before system enters S1 standby.
- Fixed issue where flashing the previous BIOS through EBU in Windows XP generated CMOS checksum errors.
- Updated from AMI Core 08.00.05 to 08.00.07.
- Added MPS support
- Fixed password is required to enter maintenance mode issue.
- Added Support for HT Technology splash logo.
- Added new BBS codes to preserve the boot order.

P05-0012

- Added the latest SATA controller BIOS OP-ROM version 4.1.45 to to enable DMA transfer modes in real mode which will improve performance significantly in DOS operations
- Added burn-in mode in Advanced\Chipset Configuration
- Fixed cache size decoding for Celeron ® processors

P03-0010

- Fixed floppy issue with floppy 3-mode enabled.
- Fixed programming default for Intel ® Precision Cooling.

P03-0009

- Changed “Clock Chip Configuration” to “Burn-in Mode”
- Corrected an issue with Burn-in Mode functionality

P03-0008

- Fixed PXE base ROM dispatching issues.
- Adding Hardware Monitoring screen for setup.
- Changed control to meet legal requirements, changed name to "Clock Chip Configuration."

P02-0007

- Removed Floppy 3 Mode support.
- Added Clock Margining support.

P01-0005

- Updated memory reference code to 1.50 with DDR 200Mhz support removed
- Fixed thermal trip detection code for MFG.
- Updated Intel Boot Agent to 4.1.08.
- Reprogrammed the SATA Controller’s class code and subsystem IDs upon resuming from S3.
- Added support for Intel ® Integrator Toolkit 2.0 and BMI 1.1.
- Fixed an issue of incorrect "Block mode" display of Secondary Slave on the IDE configuration screen.
- Added the ability to enable and disable S.M.A.R.T. hard disk drive capabilities.
- Fixed an issue where USB mouse is slow to respond coming out of S3 in Microsoft Windows* 2000.
- Updated SATA Option ROM to version 4.1.36
- Separated the functionality of "Serial ATA boot" and "Serial ATA RAID" questions in setup. They now work independently.